BECAUSE INNOVATION MATTERS™

Applied Centura® Integrated Gate Stack

In a high-k/metal gate transistor, the dielectric stack is composed of the interface oxide layer, typically grown thermally or chemically, and the bulk high-κ layer, deposited by either chemical vapor deposition or atomic layer deposition (ALD). With each node, the stack thickness must scale down to meet ever decreasing effective oxide thickness (EOT) targets to achieve desired device performance. To reduce the EOT further, plasma nitridation can be employed to incorporate a controlled dose of nitrogen into the stack, followed by annealing to stabilize it. To date, this process flow has successfully addressed performance requirements.

Extending Moore's law to the 22nm and 14nm nodes, however, poses scaling challenges. The dielectric gate stack is the core of the transistor and is electrically very sensitive to variation and quality. By adding a high-κ dielectric film to the gate stack, two additional interfaces are introduced. At the 22nm node and below, interface and queue-time control become critical factors. Perturbations in quality can be reduced by (a) having a consistent and minimal queue-time between each step and (b) keeping the wafer in a controlled vacuum atmosphere between steps. At each logic technology node reduction, the interface-to-bulk ratio increases dramatically, making elimination of queue time ever more crucial to avoid thickening of the interface layers. Also, during vacuum breaks, molecular contaminants (e.g., C, N, O, F, S) can be incorporated into the gate stack interfaces. Clustering each of the process chambers onto a vacuum mainframe is the surest way of minimizing these issues and ensuring high performance and low variability. Applied's market-leading SiON cluster tool has been in production for multiple generations.

The Centura Integrated Gate Stack system with ALD high-κ chamber technology for 22nm and below uses the same production-proven Centura Gate Stack platform to cluster the ALD high-κ process sequence in a controlled, production-worthy fashion without a vacuum break. The system incorporates our manufacturing-ready ALD HfO_2 (hafnium oxide) deposition chamber with specialized chambers for interface layer oxide formation, post high-κ nitridation, and post-nitridation anneal (PNA).

Low-temperature radical oxidation enables scaling the interface layer down to 2Å in a controlled and repeatable fashion with a thermal budget compatible with both gate first and gate last processes. Replacing thermally grown oxide dielectrics with ALD HfO_2 requires excellent uniformity and low particle count. Applied's ALD high-κ demonstrates 100% step coverage on very high aspect ratio features, confirming its extendibility to emerging 3D transistor structures.

Low-temperature plasma nitridation suppresses unwanted dielectric gate thickening caused by thermal processes, thus enabling greater EOT scaling control. While conventional plasma nitridation approaches a limit when scaling the dielectric gate to thicknesses of approximately 20Å, Applied's nitridation process can extend HfO_2 to <8Å EOT.

By providing the most production-worthy configuration for dielectric gate stack fabrication, the new Integrated Gate Stack system for 22nm and below enables significant benefits to be derived from future improvements in each of the unit processes as they occur.