Ultrathin SiO_2 Interface Layer Growth

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***Abstract*-A variety of processes based on radical oxidation (N_2O/H_2) and spike RTO are investigated in this study to grow ultrathin SiO_2 layers. Their process space is mapped out to cover regimes of interest for gate-last or gate-first integration of high k dielectrics with metal gates. Applied's Centura RTP chamber is found to be readily compatible with the requirements associated with 22/20nm CMOS technology.**

I. Introduction

Continued scaling of the gate dielectric has driven the adoption of high-k materials for the gate stack. A key challenge for enabling the adoption of these high-k materials is providing a SiO_2/SiON interfacial layer in a controlled and repeatable manner. For 28nm, a process based on radical oxidation (N_2O/H_2) has been successfully integrated with the high-k dielectric, enabling 28nm device requirements to be met. Further scaling this interface layer is now seen as critical to successfully meet the targets required for 22/20nm CMOS technology.

Meeting the interface layer thickness of less than 6Å is complicated by the need to simultaneously accommodate different process integration schemes for the high k gate dielectric and metal gate stack. SiO_2 films that are grown at high temperatures (>900°C) are preferred given that the higher temperatures result in higher quality oxide as evidenced by improved gate reliability [1, 2]. Although a gate-first process integration scheme can utilize these higher temperatures, the need to limit the growth to <6Å requires significant process control to enable a robust production-worthy process. In contrast, the thermal budget constraints associated with a gate-last process integration scheme must necessarily operate at lower temperatures (<~700°C). To satisfy the combination of temperature, thickness, and quality constraints, a variety of different processes based on extending the production-proven capabilities of Applied's radical oxidation and rapid thermal oxidation processes are investigated. These processes and their process space are mapped out in terms of temperature and thickness.

Process	Low Temp RadOx	Spike RTO	High Temp RadOx	Spike RadOx
Temp(C)	600-800	700-1000	850-1050	850-1050
Pressure	18T	1-5T	1T	1T
Time (s)	5, 60	Spike	5	Spike
Flow (slm)	20	5	5	5
Gas Comp	1% H2 in N2O	2-100% O2	2-40% H2	40% H2

TABLE 1. Summary of processes studied

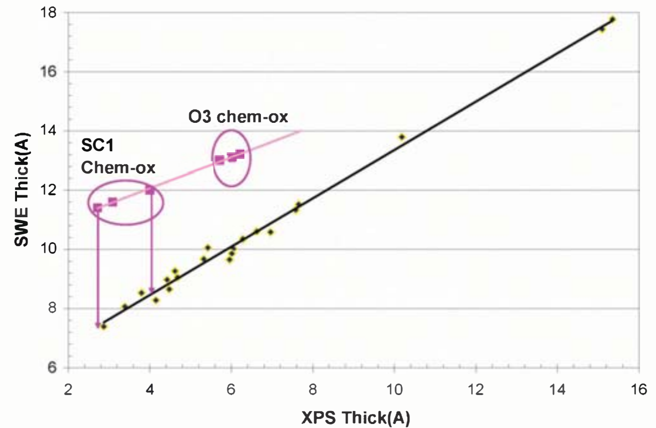

Fig. 1. Metrology correlation between ellipsometry and XPS for SiO_2 thermal oxide

II. EXPERIMENTAL

For thin SiO_2 films, surface preparation is important. An SC1-terminated ChemOx treatment was used to passivate the surface and found to be relatively uniform and stable up to 8hr

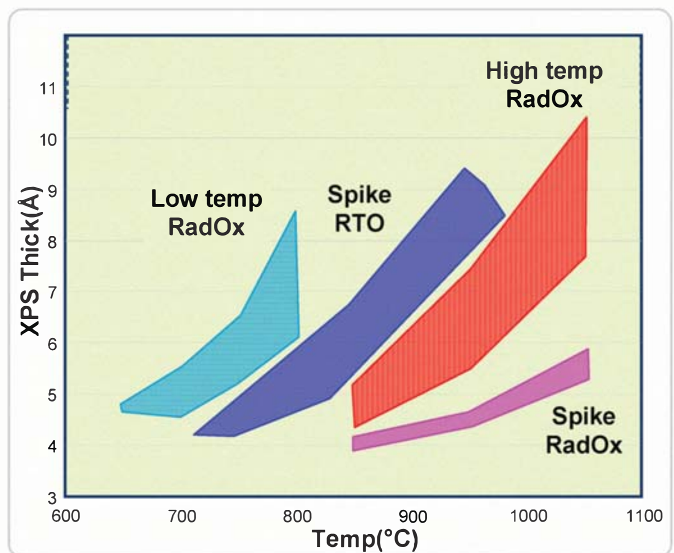

Fig. 2. Process regimes for four processes studied

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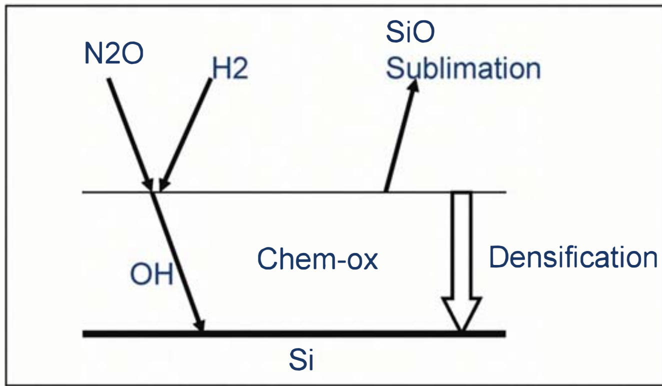

Fig. 3. Simplified mechanism for radical oxidation with N_2O/H_2

without any impact on the grown SiO_2 films. For SiO2 films <4A, an HF-last process was utilized which were stable up to 2hr. Metrology includes single wavelength ellipsometry with thermal desorption immediately before measurements and XPS (from ratio of Si 2p and SiO 2p peaks). In addition, the former was used for thickness uniformity and latter for absolute thickness and their correlation is shown in Fig. 1 for a series of thermal oxide films grown on an HF-last surface or a SC1 surface. The ellipsometry thickness is ~4Å thicker than the XPS value which is in closer agreement with TEM thickness observed in cross-sections of the gate stack. Fig. 1 also shows the chem-ox (SC1 or O_3 terminated) thickness by both metrology techniques and significantly deviates from the correlation. These films are significantly less dense than thermal oxide and SC1 has ~67% of the density of thermal oxide and are utilized for this study. HF-last was also used for a few cases.

Several processes were used and are summarized in Table 1. Radical oxidation (N_2O/H_2 RadOx) offered a wider process space that spanned both low (<700°C) and high (>800°C) temperature regimes. Spike RTO overlapped the interim regime. Spike radical oxidation was also investigated as a means for scaling.

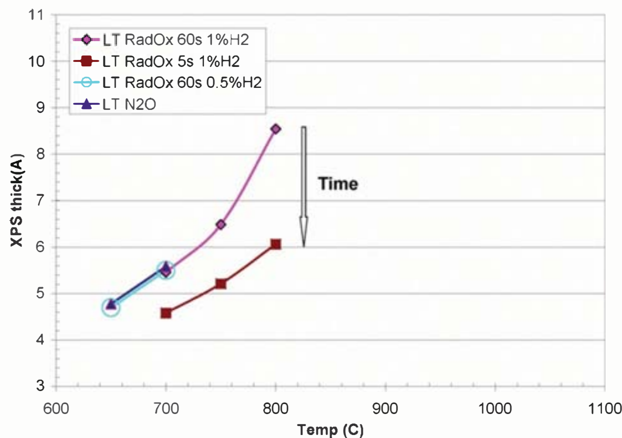

Fig. 4. Low temperature RadOx (N_2O/H_2) process window

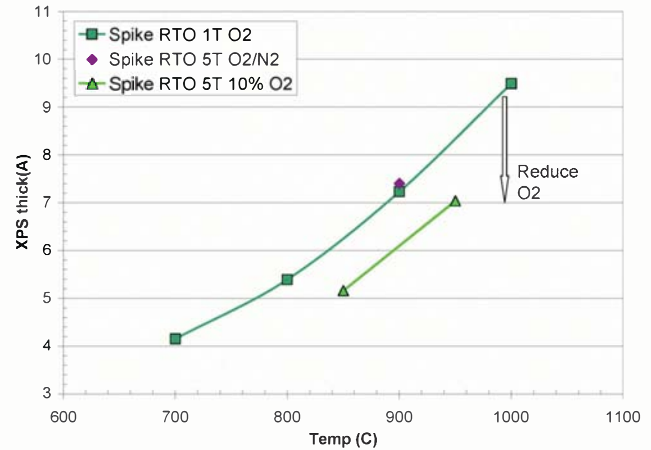

Fig. 5. Spike RTO process window

A Centura™ reduced pressure RTP system was used without any modifications to map out the process window for the temperature range 600 to 1100°C and with particular attention to the clean time window as discussed earlier. The queue time to metrology was typically <4hr as the metrology described above are less prone to air-borne molecular contaminants.

II. RESULTS

The overall process space is shown in Fig. 2 and shows the regime for each of the four processes. They will be described in detail later. Using SC1-passivation, the lower thickness limit is close to 4Å and is comparable to the starting chem-ox by XPS of ~3Å. The oxidation can be thought of a competition between oxidation, sublimation and densification as illustrated in Fig. 3, whose contributions will change across this study process window. The result is that films <4Å cannot be achieved without further reduction of the starting chem-ox thickness or requires the use of an HF-last clean.

The results for low temperature RadOx (N_2O/H_2), spike RTO and high temperature RadOx are shown in Fig. 4-6. LT RadOx is an extension of the standard N_2O/H_2 process down to low temperatures (Fig.4). Process time at each temperature can be used to tune thickness further over a 1Å

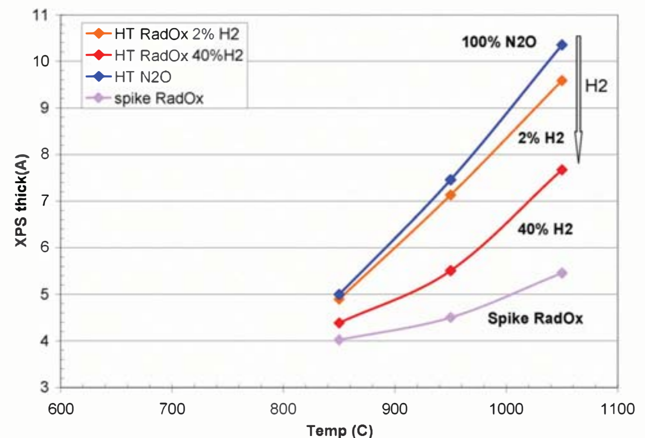

Fig. 6. High temperature RadOx (N_2O/H_2) process window

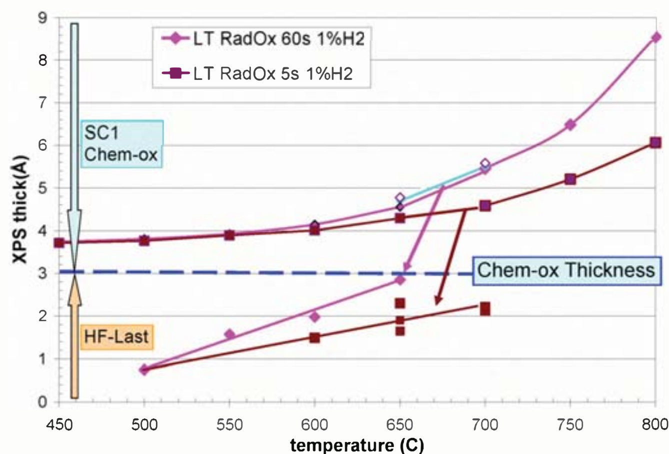

Fig. 7. Extendibility of low temperature RadOx (N_2O/H_2) process window with temperature and chemical clean

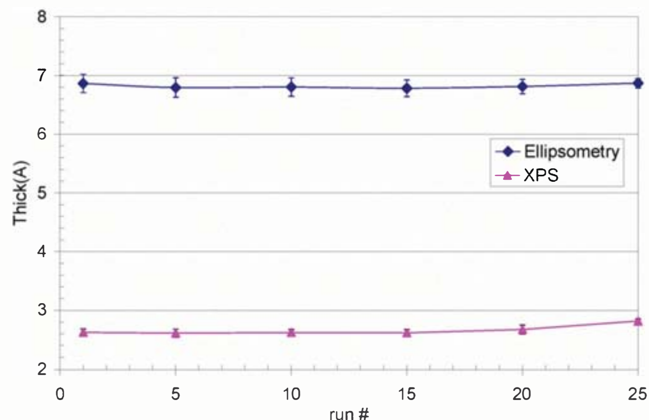

Fig. 8. Example of thickness repeatability across a 25-wafer lot for LT RadOx process at 700°C on HF-last surface

span. The lower thickness limit of 4Å is reached at ~600°C and will be discussed later. HT RadOx (Fig. 6) spans the thickness range 4 to 10Å by XPS and temperatures from 850 to 1050°C and is expanded as the elevated temperatures accentuate the three key reaction components of the oxidation process as shown in Fig. 3. The hydrogen content is the better parameter for controlling thickness at any temperature. In all cases the process or soak time is 5s and further thickness reduction is possible with a spike process, which effectively reduces the soak time (Fig. 6). As the spike is at reduced pressures, the spike width is approximately 3s. Spike RTO fills the process space between low and high temperature RadOx (N_2O/H_2) and illustrated in Fig. 5. At any temperature the thickness can be tuned using the partial pressure of O_2 whether 100% O_2 or diluted with N_2. Again the peak width is limited by the total pressure which for these studies was up to 5Torr.

In all cases where SC1 chem-ox was used the lower thickness limit was ~4Å as illustrated in Fig. 7. All processes asymptotically approach this limit and a fundamental limit with this starting oxide. Further reduction is possible by using an H-passivated surface or an HF-last clean and Fig. 7 shows that a 2Å thickness reduction is achieved. The physical limit for XPS is ~1Å. By using an HF-last clean, this 2Å thickness reduction is achieved across most of this process space.
To illustrate the repeatability of any of these processes, Fig. 8 shows an example of a 3Å process applied across a 25-wafer lot and includes error bars for within wafer uniformity.

By simple extensions of radical oxidation (N_2O/H_2) SiO_2 deposition is possible down to a thickness of interest for interface layers for high k scaling at 22/20nm CMOS node.

REFERENCES

[1] C. S. Lai et al, ISDRS 2007.
[2] T-M Pan et al, IEEE Electron Device Lett., vol 23, p 416, 2002