High-k / Metal Gate Stacks in Gate First and Replacement Gate Schemes

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Abstract **- In this work, representative high-k/metal gate MOS-capacitor stacks were fabricated in both gate first and replacement gate integration schemes. Aluminum- and lanthanum- based cap layers (both widely accepted as Vt tuning cap layers in the industry), in addition to TiN metal gate, can tune the effective workfunction towards PMOS and NMOS, respectively. Varying Ti:N stoichiometry in TiN can induce >250mV change in TiN workfunction. 1 volt separation between NMOS and PMOS was achieved by screening various workfunction materials in replacement gate scheme. Substrate modification during the growth of aluminum was key to achieving void-free aluminum gap fill in narrow gate trenches.**

1. INTRODUCTION

Scaling down of metal-oxide-semiconductor field-effect-transistor (MOSFET) devices beyond 50nm requires a High-*k* metal gate (H*k*MG)-based gate stack to address high gate leakage and the reduction in gate capacitance due to poly-silicon gate electrode depletion issues. Implementation of H*k*MG is challenging and requires gate workfunction tuning to control threshold voltage (V_t) using new materials and integration schemes. To navigate these complexities, two main integration schemes were suggested – gate first (GF) [1-5] and replacement gate (RG) [6-10]. Gate first scheme, which is similar to the SiON/Poly process flow, requires the H*k*MG stack to withstand S/D activation anneal, maintain stable leakage-effective oxide thickness (J_g-EOT) scaling and enable workfunction tuning. Compositional tuning of the metal gate film and inclusion of a "cap layer" between the high-*k* and metal gate remain the popular means of achieving the desired workfunction in the gate first scheme [11-14]. In the case of replacement gate, V_t tuning can be achieved by selecting appropriate workfunction metals. With the strain-enhancement techniques like embedded S/D SiGe, poly-silicon removal step during replacement gate process was shown to offer at least 50% increase in lateral compressive stress in the channel [8,9]. This strain enhancement results in improved hole mobility making replacement gate ideal for high performance (HP) devices. In this scheme, gate trenches after the workfunction metal deposition need to be filled with a low-resistance metal, like tungsten [6] or aluminum [10]. This paper describes the testing of key concepts in both integration schemes like – flat band voltage (Vfb) tuning with cap layers and metal electrode in gate first scheme, workfunction screening of probable metal electrodes and a pathway for extending the aluminum gap fill, in replacement gate scheme.

2. EXPERIMENTAL

The detailed process flow of MOS-fabrication was shown in Figure-1. Al-based (PMOS) and La-based (NMOS) cap layers were used for the V_t tuning of hafnium oxide (HfO_2) and hafnium silicate (HfSiOx) high-k and titanium nitride (TiN) metal gate, in the gate first scheme. Several materials were screened for their workfunction in the replacement gate flow. Aluminum gap fill work was done with a ultra high vacuum-integrated PVD titanium wetting layer followed by an aluminum seed layer and high temperature reflow (Figure No. 2).

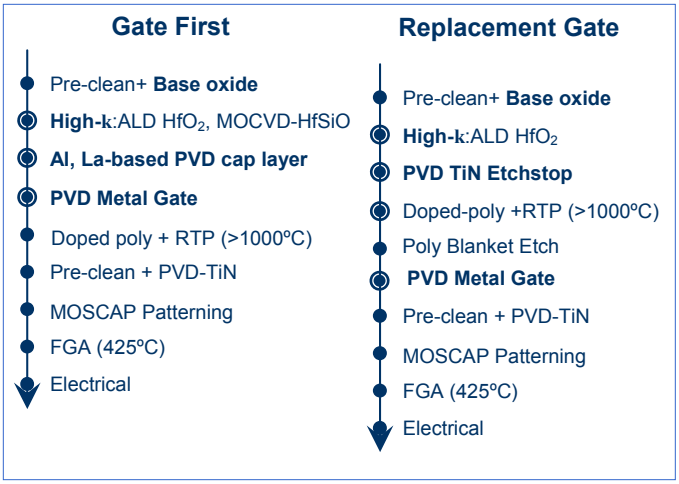

Figure-1: MOS-fabrication flow used for GF and RG flows. Two integration flows were used in RG – high-k first/metal last and both high-k last/metal last.

3. FLAT-BAND VOLTAGE TUNING IN GATE FIRST SCHEME

Changing the Ti-N_2 stoichiometry from Ti-rich to poison mode induced ~265mV V_{fb} shift towards PMOS (Figure No. 3). This is in agreement with previous findings [5]. Changing the N_2 content on TiN film also resulted in EOT variation as shown in Figure No. 3. This behavior is attributed to (a) the manipulation of k-value of the high-k film due to the abundance of Ti and nitrogen in Ti-rich and poison stoichiometries and (b) physical growth of the interface layer (IL) during the high-temperature anneal caused by diffusing nitrogen and oxygen species in the high-k. Addition of 5-10ÅLaO_x cap layer resulted in large (>500mV) V_{fb} shift

towards NMOS (Figure No. 4). The shift achieved by PVD-TiN#2 (poison-mode) is less towards NMOS compared to that achieved by PVD-TiN#1 (metallic-mode). This is consistent with the HfO_2/TiN Vfb data shown in Figure-3. Hence, both TiN stoichiometry and La-dosage can be optimized to achieve the desired V_{fb} shift. Similar study using 7Å AlOx on a HfSiON/TiN stack showed higher Vfb shift (180mV) on a metallic mode TiN compared to a poison-mode TiN (60mV) (Figure-5). However, the net Vfb of AlOx/TiN stacks were same in both cases.

4. WORKFUNCTION SCREENING IN REPLACEMENT GATE SCHEME

Figures No. 6 (PMOS) and No. 7 (NMOS) illustrate the workfunction screening data of prospective metal electrodes for NMOS (ALD HfAl, PVD HfC, PVD TiAl) and PMOS (ALD WN, ALD RuO, PVD TiN) in the replacement gate scheme (high-k first, metal gate last with HfO_2 high-k dielectric). PVD TiAl and PVD TiN come close to band edge with effective workfunction (eWF) of 4.1 eV and 4.85 eV, respectively. The C-V curves of HfO_2/PVD-TiN and HfO_2/PVD-TiAl stacks ran in the same flow showed a 1 volt separation in V_{fb} between NMOS and PMOS indicating band-edge workfunction for these metal films (Figure No. 8). C-V curves also indicate good with-in-wafer uniformity of both V_{fb} and EOT for the deposited stacks.

5. ALUMINUM GAP FILL STUDIES

The Step coverage of PVD-Ti wetting layer is critical for aluminum wettability and void-free gap fill. This was enhanced in an ionized-PVD chamber by increasing the substrate bias. Higher substrate bias condition (1000W bias compared to 550W) resulted in a superior gap fill, as shown in Figure No. 9. Isotropic growth of CVD Al seed layer, in addition to the overhang at the top of the trench from previously-deposited PVD layers, often results in pinch-off and a fill void at the center of the trench. Growth of CVD Al growth was inhibited by surface modification of the top-portion of the trenches with nitrogen treatment. This avoided pinch-off at the top of the trench and resulted in enhanced bottoms up fill in narrow (<20nm top CD) trenches, as shown in Figure No. 10.

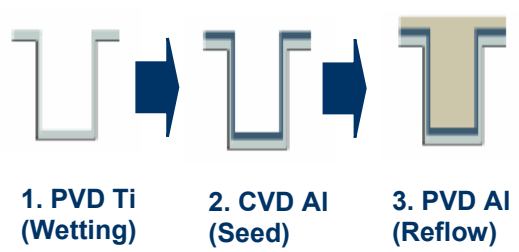

Figure-2: Process flow of Al gap fill containing Ti wetting layer, Al seed and reflow layers.

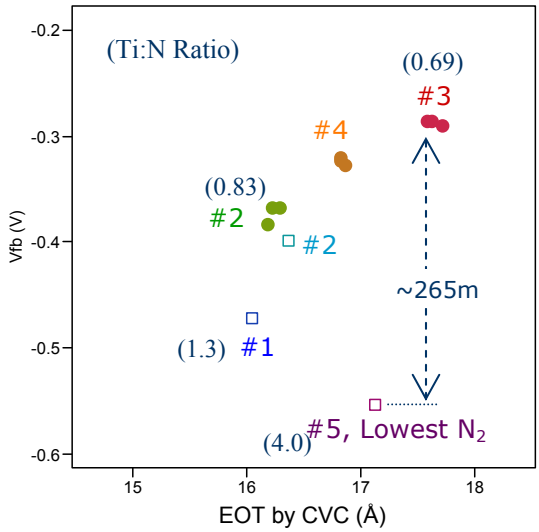

Figure-3: Impact of Ti:N_2 stoichiometry on flatband voltage of HfO_2/TiN stack layers in gate first integration

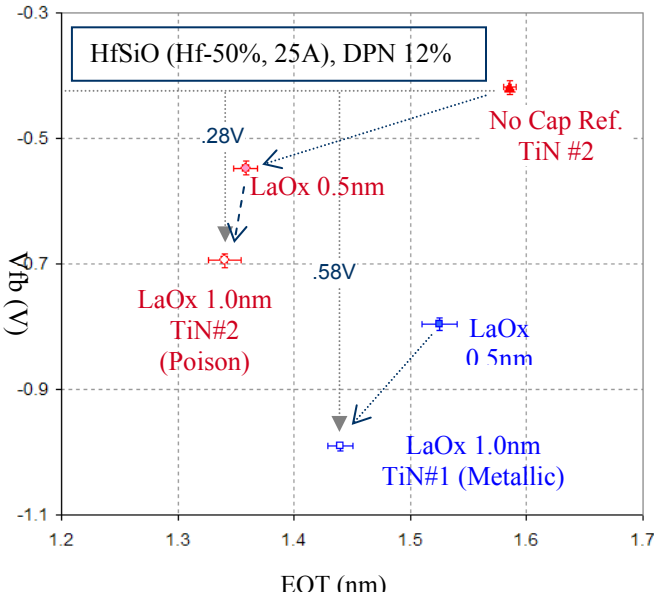

Figure-4: Flat-band voltage (V_{fb})-EOT of LaO_x/TiN stack in gate first scheme. TiN#2 is poison mode TiN.

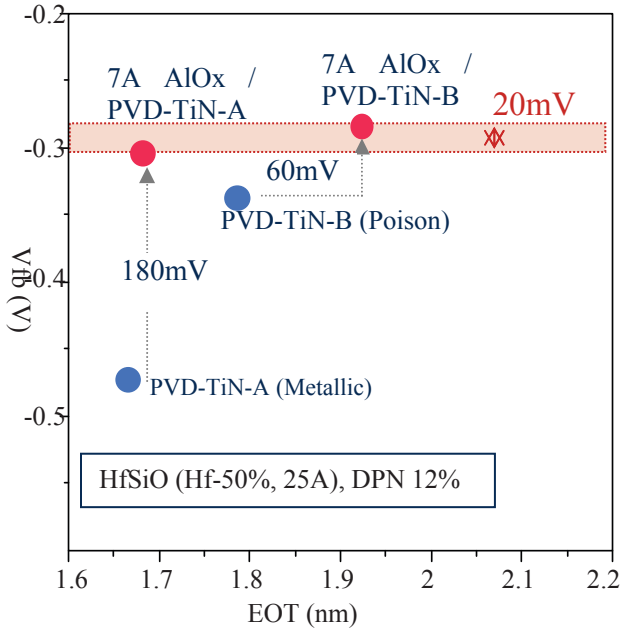

Figure-5: Flat-band voltage (V_{fb})-EOT of AlOx/TiN stack in gate first scheme.

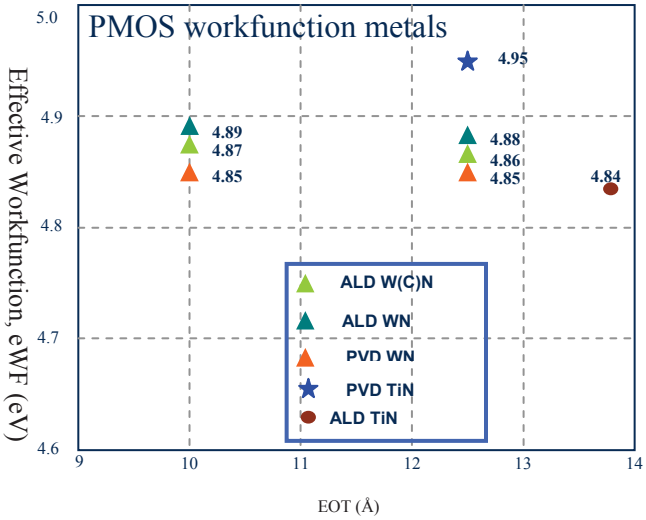

Figure-6: Workfunction screening of PMOS metals in replacement gate (high-k first, metal gate last) integration flow

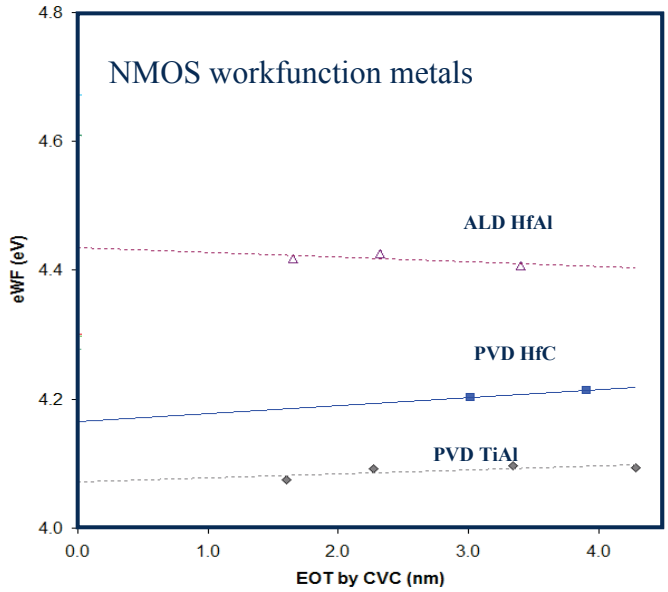

Figure-7: Workfunction screening of NMOS metals in replacement gate (high-k first, metal gate last) integration flow

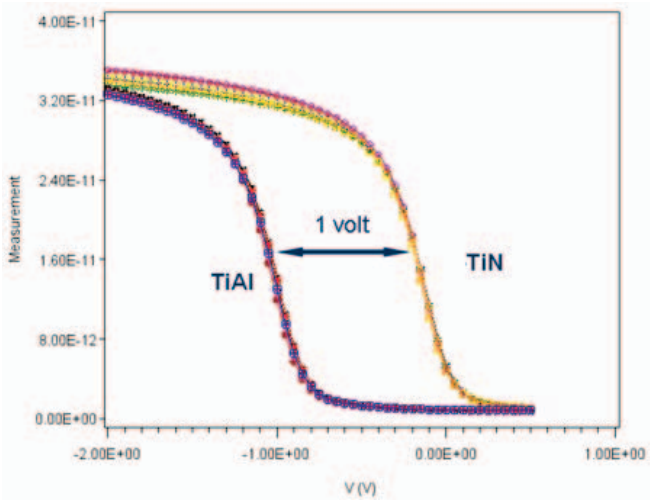

Figure-8: C-V measurements of TiN (PMOS) and TiAl (NMOS) deposited in replacement gate scheme showing 1 volt separation. Muliple curves per condition represent with-in wafer uniformity of the stack films.

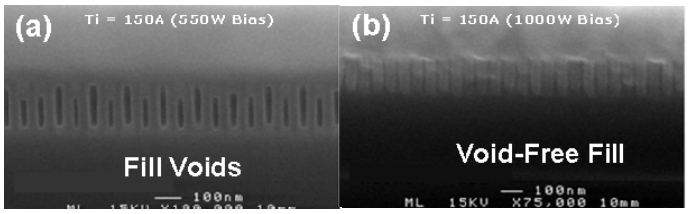

Figure-9: Impact of substrate bias of PVD Ti wetting layer on gap fill

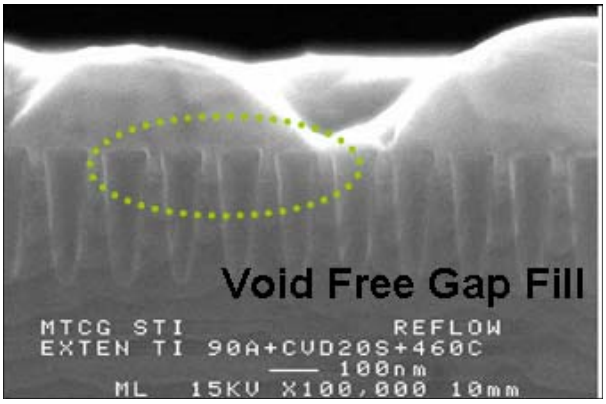

Figure-10: Void-free Al gap fill achieved by preferential liner treatment of PVD Ti wetting layer in N_2 plasma

6. CONCLUSIONS

High-k/metal gate MOSCAP structures were fabricated in gate first and replacement gate integrations and the resultant V_{fb}-EOT and workfunction data were reported. AlOx, LaOx cap layers, along with the right TiN stoichiometry showed a Vfb shift of >200mV in gate first flow. 1 volt separation between NMOS and PMOS V_{fb} was achieved by TiAl and TiN metal gate electrodes in replacement gate integration. High-bias during wetting layer deposition and preferential liner treatment concepts were reported for extending aluminum gap fill in narrow trenches.

7. REFERENCES

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