Through-Silicon Via 3D Integration

Introduction

Semiconductor devices are constantly responding to the demand for "faster, cheaper, smaller." Devices are expected to deliver more functionality at greater speed in smaller dimensions as consumer electronics become increasingly complex and more compact. In the past these demands have largely been met through miniaturization of circuits and their components. However, in recent years 3D integration in the form of wire bond and flip-chip stacking has made its way into mainstream semiconductor manufacturing to address the limitations of physical scaling while delivering greater performance and functionality.

Now "through-silicon via" (TSV) is emerging as a method of 3D integration that offers designers more freedom, and greater energy and space efficiencies than wire bonding and flip chip stacking. TSV is expected to enter the mainstream in 2010, especially for memory devices. This paper is a basic introduction to TSV technology, associated implementation challenges, and the steps Applied Materials is taking to enable TSV for commercial production.

TSV: The Basics

3D integration describes the process of vertically connecting several chips to achieve high functionality-to-volume ratio using established silicon technology and micro fabrication methods.

In TSV, two or more vertically stacked chips are joined by vertical interconnects running through the stack (i.e., across the interface between two or more adjacent chips) and functioning as components of the integrated circuit. Stacking and connecting (similar or different) die enables the creation of high-performance devices made from components fabricated at non-leading edge geometries.

While two die could be combined using conventional wire bonding techniques, the inductive losses would reduce the speed of data exchange, in turn eroding the performance benefit. TSV addresses the data exchange issues of wire bonding, and offers several other attractive advantages. For example, TSV allows for shorter interconnects between the die, reducing power consumption caused by long horizontal wiring, and eliminating the space and power wasted by buffers (repeaters that propel a signal through a lengthy circuit). TSV also reduces electrical parasitics in the circuit (i.e., unintended electrical effects), increasing device switching speeds. Moreover, TSV accommodates much higher input/output density than wire bonding, which consumes much more space.

TSV Applications

TSV will eventually be used in both homogeneous and heterogeneous integration. In homogenous integration, die of the same type are connected; in heterogenous integration, die of different types are connected.

Memory makers will implement homogenous TSV integration to produce stacked DRAM to boost the memory capacity per unit board area, thereby reducing PC board costs. This method reduces latency and increases bandwidth between memory and processor.

Applications for heterogeneous integration include image sensors or communication chips in cell phones stacked with DSP and memory; and schemes for gaming systems. Heterogeneous integration enables faster data exchange between the sub-components compared to other 3D integration techniques.

The most immediate demand for TSV is in image sensors. However, while image sensors have led the way in unit volume produced on 200mm wafers, this market does not constitute high volume today in terms of wafer starts. Cumulative volumes will be significantly larger when TSV goes mainstream at 300mm for stacked memory and integrated logic/memory chips. Longer term, with the continued evolution and increased sophistication of MEMS devices, TSV will be implemented in these as well.

Challenges to TSV Implementation

Cost

Implementation cost, determined by numerous aspects of design and manufacturing, is the biggest barrier to broad commercialization of TSV technology. In particular, the current major cost barriers to TSV are bonding/de-bonding and via barrier/fill, as explained below.

The value of TSV can be tremendous once production costs fit the roadmap. For example, today's smart phones integrate an RF base band chip, Flash memory, and an ARM processor onto plastic at a cost of approximately $12-17. Heterogeneously integrating these chips using TSV could cut integration costs to well under $5.

The industry currently considers a 30% cost increase (over wire bonding) to be acceptable for TSV, given TSV's much higher return in functionality and performance. This equates to a target cost-per-wafer below $150 for 300mm substrates.

Design

As TSV is adopted in increasingly complex applications that combine different types of chips, design guidelines and software must keep pace to address a variety of issues. With several thousand interconnections between die, chip architecture and layout must undergo fundamental changes. Designers for each chip type used in the integration scheme will have to leverage the same master layout to line up connection points between the chips. At the same time, designers will need to consider possible heat generation issues. Stacked chips may overheat if some thermal management mechanism is not included in the design. Hot spots and temperature gradients strongly affect reliability. Conventional two-dimensional (2D) thermal management techniques will not be adequate for 3D problems; more sophisticated solutions will be required.

Manufacturing

For greatest cost-effectiveness, the full manufacturing sequence requires seamless integration and optimization between traditional steps in wafer processing and back-end packaging. The entire flow must be optimized to deliver the greatest performance (yield, reliability) for the highest productivity (cost).

In TSV applications, the process sequence differs, depending on whether the via first or via last approach is used (as addressed below). In either approach, the TSV stack undergoes bonding, thinning, wafer processing on bonded/thinned wafers, and subsequent de-bonding. Wafers are typically bonded to carriers (glass or dummy silicon) and thinned down to a thickness ranging from 30 to 125µm. This introduces new manufacturing challenges, including thermal budget control. To preserve the adhesive integrity of the bonding material once wafers are bonded, processing temperatures cannot exceed 200°C.

Another manufacturing challenge is the need for new automatic test capabilities compatible with 3D integration to ensure electrical functionality of the finished devices.

Chip stacking can be die-to-die (chip-to-chip), die-to-wafer or two whole wafers stacked together. For early mainstream applications, die-to-wafer integration will be most common, involving the stacking of a single Known Good Die (KGD) onto a KGD on a wafer. Wafer-to-wafer integration will become more common only as consistently high yielding wafers are produced.

TSV Processes and Integration

Via Creation

Vias for TSV 3D integration were initially created using laser ablation. However, with the increase in the number of vias and concerns regarding damage and defects, deep reactive ion etch technology, well proven in traditional semiconductor manufacturing, has become the process of choice. Depending on application, a via first or via last process sequence is followed.

Via First: Vias are etched during front-end-of-line processing (i.e., during transistor creation) from the front-side of a full-thickness wafer. This approach is favored by logic suppliers and is the most challenging by far. The smallest via diameters for via-first schemes tend to be 5 to 10µm; aspect ratios are higher (10:1), posing challenges for liner and barrier step coverage, and for the quality of copper fill.

Via Last: Vias are etched during or after back-end-of-line processing (i.e., interconnect formation) from the front-side of a full-thickness wafer or backside of a thinned wafer. This approach is used in image sensors and stacked DRAM. CMOS image sensors have via diameters exceeding 40µm with aspect ratios of 2:1. In other devices, the vias range from 10 to 25µm with aspect ratios of 5:1.

The biggest challenge in via creation is to etch extremely fast with good profile control, maintaining a low cost of ownership (CoO). Leveraging Applied Materials' extensive experience in deep silicon etch for aspect ratios as high as 80:1 and in running 200mm TSV production for CMOS image sensors, the **Applied Centura® Silvia™ Etch** combines the fastest etch rate available with the best profiles for deep silicon etch at the lowest CoO. Using a proprietary process that overcomes the historical tradeoff between etch rate and profile roughness, the Centura Silvia Etch system performs equally well for both via first and via last applications.

Via Liners

To avoid shorting to the silicon, the etched vias must be lined with an insulating layer of oxide (dielectric) before being filled with metal. If a copper fill is used, a second metal barrier liner is also needed. Copper will most likely be used in mainstream applications for its conductivity and cost benefits.

Chemical vapor deposition processes are ideal for TSV dielectric liner applications because of their inherently conformal deposition. Conformality is critical for good step coverage in the subsequent titanium metal barrier and copper seed steps. With the high-productivity **Applied Producer® InVia™ system**, Applied Materials offers a highly conformal process for depositing robust insulating liners for high aspect ratio via-first and via-middle TSV applications. The InVia film possesses good breakdown voltage and leakage current properties with excellent adhesion to the industry standard barrier metals (Ta, Ti and TaN/Ta). Applied's plasma-based processes are ideal for integration schemes where thermal budget considerations are critical, producing oxides and nitrides that combine high quality film properties and low-temperature (~200ºC) deposition.

Depositing the barrier layer and subsequently filling the via with metal are among the most challenging and expensive processes in the TSV flow. Titanium or tantalum are favored as barrier materials for copper TSVs just as they are for advanced logic devices in which good step coverage is also essential. These materials are deposited using physical vapor deposition (PVD) processes for which Applied's most advanced system, the **Applied Endura® Extensa™ PVD**, delivers highly uniform step coverage and sheet resistance, allowing a thinner barrier to be deposited to promote void-free metal fill. The system delivers the industry's best defect performance and operates at 25% lower cost of consumables than other available barrier deposition systems with thinner film also helping to lower the cost of ownership per wafer.

Via Fill

Experiments have been performed using tungsten and polysilicon as the conductive fill material for TSV vias, especially for the via-first approach. However, both tungsten and polysilicon do not conduct as well as copper and hence copper fill is the mainstream approach today. For via fill with copper electroplating, Applied is partnered with Semitool to develop integrated process sequences to jointly optimize etch, dielectric liner, barrier/seed, and plating steps.

Chemical-Mechanical Polishing
Depending on the TSV processing sequence adopted, chemical-mechanical polishing (CMP) can be used to remove oxide or metal. Challenges include rapid removal of thick materials at low CoO without compromising wafer topography. Applied has years of CMP experience with its **Applied Reflexion®** family of products.

Bonding, Thinning, De-Bonding, and Wafer Handling

Temperature control, electrostatic chucking, chemical compatibility, and mechanical handling are other key factors that need to be fully characterized prior to TSV reaching high volume production. Applied Materials is working closely with suppliers and customers to ensure that optimum substrate technology can be validated on a standard wafer fab processing tool.

Applied Materials' TSV Module

As a leader in proactively advancing technology to enable customer roadmaps and address challenges, Applied Materials is leveraging its broad range of assets (technology, integration expertise, equipment and supplier relationships, and the Maydan Technology Center) to accelerate implementation of TSV in mainstream production. Applied's approach is three-fold:

- Boosting Unit Process Output and Yield: Applied is characterizing inter-process dependencies (such as etch profiles and via fill rates) to optimize the tradeoffs between *performance and productivity*.
- Reducing Customer Development Time and Risk: Applied is completing early cycles of learning on full process flows, and validating electrical and structural properties in our Maydan Technology Center.
- Leading the Industry in Cost-Effective Integration: Applied is collaborating with materials, equipment, and packaging suppliers (such as Semitool for electrochemical plating) to ensure full TSV process readiness at an affordable cost. By focusing on the TSV formation steps and working with bonding/thinning suppliers, Applied is concentrating on optimizing steps that account for over 65% of the total costs.

Working together across the industry, Applied's goal is to qualify an end-to-end process flow that offers the most cost-effective approach to commercializing TSV technology and accelerates customers' time to market.