

## Mitigating eSiGe Strain Relaxation using Cryo-implantation Technology for PSD Formation

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**Abstract** - Strain techniques have been adopted and widely used in the advanced nodes since early 65nm for carrier mobility improvement. For PMOS, eSiGe incorporation in the SD is the process of choice to induce compressive strain in the channel for mobility improvement. To further lower the contact resistance, it is preferred to boost Boron concentration for pSD formed by eSiGe process. Normal implant process could lead strain relaxation caused by implant damage. In this paper, cryo-implantation technology is applied and characterization of strain relaxation is conducted using a state-of-the-art 28nm CMOS process flow. Experimental results indicate strain relaxation can be reduced with cryo implants relative to the room temperature implants. This study clearly showed that cryo-implantation reduced damage formation resulting in junction leakage reduction.

**Index Terms:** Novel process technology, ion implantation, cryo implant, strain relaxation

### I. INTRODUCTION

For advanced CMOS technology nodes, strain engineering has become an increasingly important technique to enhance the performance of transistors. For strained channel pMOS devices, a uniaxial compressive stress in the channel is induced by the Selective Epitaxial Growth (SEG) of SiGe in recessed source/drain (S/D) regions. Higher channel stress levels and lower S/D resistance can be achieved by increasing the Ge content and the epilayer thickness in the S/D regions [1-3]. To be fully incorporated into CMOS technology, these layers will experience and have to withstand further processing, i.e. ion implantation and annealing. It has been demonstrated that strained SiGe relaxes via misfit and threading dislocation propagation after high temperature post annealing [4,5].

In eSiGe technique, eSiGe proximity to channel is the dominant parameter for increasing channel strain. From the point view of parasitic resistance, in-situ Boron-doped eSiGe with S/D implantation provide better performance, but tends to degrade short channel behavior at close eSiGe proximity structure [6]. To achieve better activation and avoid the channeling from implantation, the Pre-Amorphization Implant (PAI) is applied during pSD formation. The End of Range (EOR) defects which are known to form around amorphous / crystalline (a/c) interface during the thermal annealing can serve as nucleation sites for dislocation formation or aid in the inter-diffusion of Boron and Ge. This can accelerate the strain relaxation. The benefits of increasing Ge content for higher strain will be vanished from the induced strain relaxation. This will lead to a lower hole mobility and higher junction leakage which can significantly degrade the device performance.

Cryo-implantation has been recognized as a way for damage engineering to address or mitigate implant damage caused detrimental effects on device performance [7]. The effects from cryo-implantation (-100°C), using Varian Process Temperature Control II (or PTC II), can be observed in the cross sectional TEM images as shown in Fig.1 for Boron 2keV, 3e15/cm<sup>2</sup> relative to the Room Temperature (RT) implant. It can be seen that cryo implant results in thicker amorphous layer with smoother a/c interface.

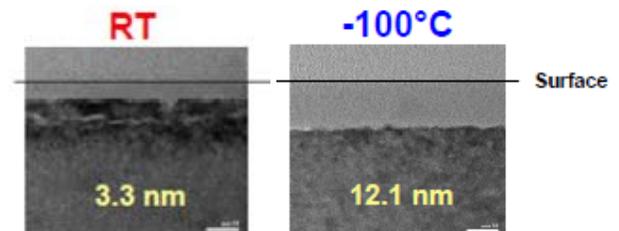


Fig. 1. Cross sectional TEM images for implant with Boron 2keV 3e15/cm<sup>2</sup> at RT and cryo temperature implants. Thicker amorphous layer with smoother a/c interface are observed with cryo implant.

In this paper, high Ge % embedded SiGe integrated with the state-of-the-art 28nm CMOS device flow are used to investigate for cryo implant effects on strain relaxation. The strain relaxations can be correlated to the mobility degradations. The junction leakage increases related to the defect propagated from SiGe layer to Si substrate after millisecond (msec) Laser anneals (LSA) are discussed. The cryo temperature p-type SD (pSD) implants to minimize the strain relaxation are demonstrated for junction leakage reduction and mobility improvement.

## II. EXPERIMENTAL

The recessed SiGe S/D junction was fabricated and integrated with the device flow as described in Fig. 2. The p/n junction was formed by in-situ doped SiGe EPI process and implantation after SiGe deposition. The implant conditions for pSD into eSiGe including different Ge PAI energies + Boron low energy, high dose SD implants and combining with implant temperature splits for both.

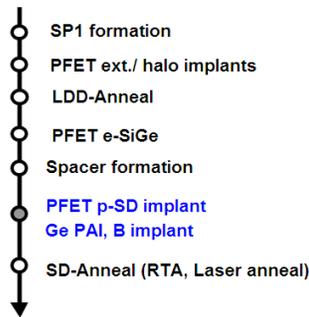


Fig. 2. 28nm pFET device flow with advanced stress formation and anneals for device evaluation and leakage measurements. Cryo-implants for pSD were evaluated along with RT control.

Spike rapid thermal process (RTP) and msec LSA anneal were applied to recover the damage induced by implant, and activate the dopants. The HRXRD (High Resolution X-Ray Diffraction) rocking curves have been employed to characterize the SiGe strain relaxation induced from implantation. This study includes 1) step by step partition for the strain relaxation after each step, including SiGe EPI, S/D implantation, Spike RTP, and msec anneal; 2) reduced Ge PAI energies (Condition #A, #B and #C with energies #A>#B>#C); 3) comparing the RT vs PTC II with both Ge and Boron implants. Secondary Ion Mass Spectroscopy (SIMS) was used for dopant profile measurements.

## III. RESULTS AND DISCUSSIONS

Fig. 3 shows the HRXRD rocking curves measured after eSiGe deposition, S/D implant, Spike RTP anneal, and msec

anneal. The broadening of Si peak indicates the extend of strain relaxation. The strained silicon peak appears on the right of the high intensity silicon peak and the relaxed SiGe is to the left. The strain levels can be determined from the peak positions. The greater the distance between the Si and relaxed SiGe peaks, the higher the strain in the Si layer. The FWHM (Full Width at Half Maximum) of rocking curve peaks are inversely related to the thickness of film layers and defects within the layers. As shown in Fig. 3, for the as-grown strained SiGe EPI sample, a fringe pattern is clearly seen around the SiGe peak, indicating there is almost no misfit dislocation is generated at the SiGe/Si interface and maintained its original strain and crystallinity. After pSD implants, the rocking curves showed relaxed SiGe peaks shifted to the left with lower peak high. Rocking curves after spike RTP and msec anneal showed much broader peaks with peak positions shift to the right. At the same time, the Si peak also showed broadening and much larger FWHM after msec anneal. This indicates that ion implant induced defects act as dislocation sources which result in aggregated strain relaxation of the SiGe layers.

Fig. 3 clearly showed that the most of strain relaxations were resulted from the re-crystallization after Spike RTP anneal step following pSD implant. The msec anneal makes strain relaxation even worse similar to the previous studies [5]. The SiGe/Si interface quality and the strain relaxation are determined from the residue defects after spike RTP anneal and the msec anneal. Post SiGe implant with different Ge implant energies will introduce varying degree of strain relaxation from different damaged SiGe layer toward the SiGe/Si interface after post implant re-crystallization anneal. Higher the Ge content in SiGe also will enhance the propagation and forming the dislocation defects.

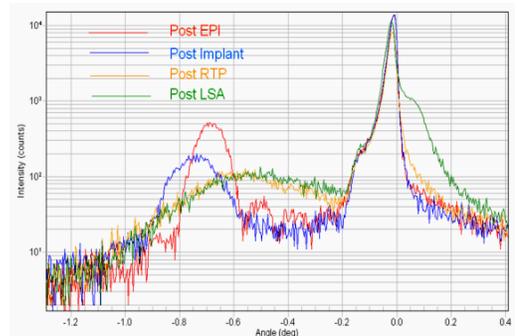


Fig. 3. HRXRD rocking curves after SiGe EPI, S/D implant, Spike RTP, and msec anneal for SiGe strain relaxation.

Fig. 4 is the strain relaxation data collected after RTP/LSA anneal relative to strain obtained immediately after SiGe EPI and before pSD implant (data were normalized). For the same Ge energy, such as Ge conditions #A or #C + Boron, the implants performed at cryo temperature showed significant less strain relaxation relative to RT implants. It is clear that Ge implant energies can

induce a significant strain relaxation. The results showed Ge lower energy (condition #C) will induce much less strain relaxation. As HRXRD rocking curves shown in Fig. 5, the strain relaxation can be recovered if comparing patterns with condition #C relative to condition #B in Fig. 3. With the cryo temperature PAI implant, the strain relaxation can be further improved.

Interestingly, the cryo implant applied on, even with just either Ge condition #C or Boron, there are some strain relaxation reduction observed comparing RT cases. With both Ge condition #C and Boron implanted at cryo temperature, strain relaxation showed even better performance. As reported previously [7], the cryo temperature PAI implant can reduce EOR damage and produces deeper amorphization and a much smoother a/c interface which can mitigate damage caused strain relaxation after thermal process. Compare to normal RT pSD implant into eSiGe, the dynamic annealing process of interstitials and vacancies generated by the implant can be retarded when the substrate temperature can be controlled significant lower. At cryo-temperature, the interstitials and vacancies will be much localized and interstitial or vacancy clusters formation will be reduced, resulting in deeper amorphization and less end of range defects [8,9].

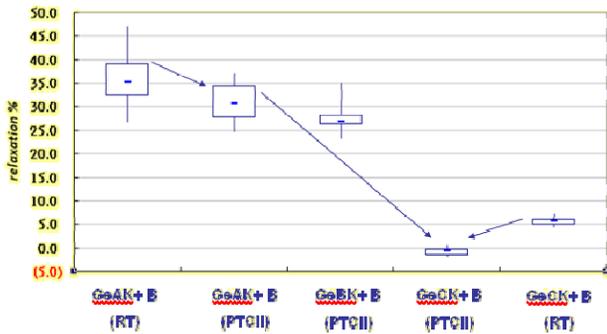


Fig. 4. Summary of strain relaxation data after anneal (RTP/LSA) relative to pre-implant strain with splits of Ge energies (#A>#B>#C) and Boron at RT and cryo temperature (PTCII). The data was normalized relative to RT Baseline (Ge #A + Boron at RT).

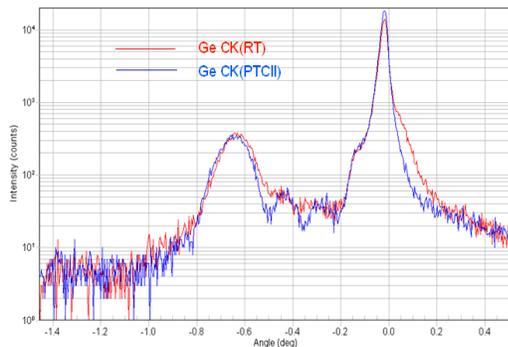


Fig. 5. HRXRD rocking curve comparison using Ge condition #C for PAI implants at RT and cryo temperature (post LSA).

Fig. 6 is the defect concentration profile extracted from 2D TCAD studies for Boron 2keV implants at either RT or cryo temperature. It is clearly shown the reduction (~4x) of defect concentration peak for cryo-implant after thermal process. It has been proved that the surface defects and end of range defects can be reduced with implants at cryo-temperature [7,9]. Indeed, the HRXRD showed the significant strain relaxation reduction from the cryo temperature implant conditions (Figs. 3-5).

To further understand the effect of strain relaxation from different implant conditions, SIMS measurements were performed on the test pads which exposed the same process flow as the HRXRD structure. Fig. 7 shows the Boron SIMS comparison between RT and cryo temperature for both Ge condition #A + Boron implants. Fig. 8 shows the Boron profiles comparison with a combination of RT and cryo temperature for Ge condition #C and Boron implants. The in-situ doping Boron at  $2e20/cm^3$  can be clearly observed with current process. With additional pSD implants, the surface Boron concentration can be raised to as high as  $2e21/cm^3$ . The diffusion of Boron is enhanced by the presence of excess interstitials induced by implant after annealing. For Figs. 7 and 8, the SIMS profile broadening at the tail regime indicates enhanced diffusivity due to Transient Enhanced Diffusion (TED). It is clear that with cryo implants either for Boron or for both Ge condition #C + Boron, there is no significant tail difference. In the meantime, the strain relaxation can be reduced further for cryo temperature applied on both implants.

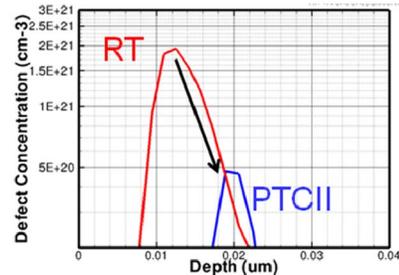


Fig. 6. The defect concentration profile extracted from TCAD studies for Boron 2keV,  $3e15/cm^2$  at either RT or cryo temperature. The defect concentration peak can be reduced by ~4x with PTCII.

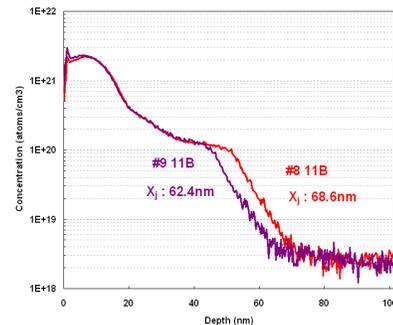


Fig. 7. Boron SIMS profiles comparison between RT (#8) and cryo (#9) temperature for both Ge condition #A + Boron pSD implants.

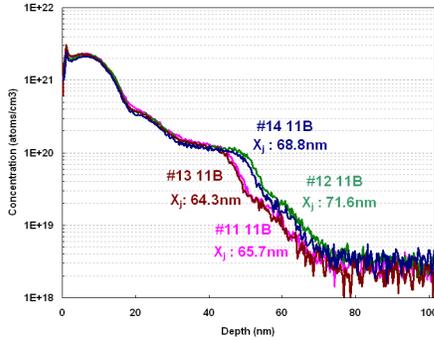


Fig. 8. Boron SIMS profiles comparison at a combination of RT and cryo temperature for Ge condition #C + Boron (cryo applied on: #11 both, #12 none, #13 B only, or #14 Ge only).

The junction leakage for different S/D implant conditions are shown in Fig. 9. In case of eSiGe S/D junction, the leakage current generated in the silicon substrate increases with the lattice misfit defects, junction profile changes from dopant distribution and from the band gap reduction [10]. Since the Ge concentration is kept as constant for all the samples used in this study, the effect of band gap reduction can be eliminated for the leakage comparisons. Interestingly, the cryo implant can result in ~6nm shallower junction (Fig. 8) compared to RT implant and therefore higher leakage current would be expected due to the higher doping density caused higher electric field and higher trap-assisted tunneling factor. Fig. 9 shows the lower leakage from cryo implant than RT control. It can be explained using defect related mechanism. Relaxation of the misfit strain can generate misfit dislocation and threading dislocation which may propagate into the depletion region in the silicon substrate, and thus increase the leakage current by reducing the generation lifetime [10]. The cryo implants can minimize leakage current due to less defects in Si substrate. Finally, the benefit of cryo implant on strain relaxation has demonstrated in the mobility improvements and will be discussed elsewhere.

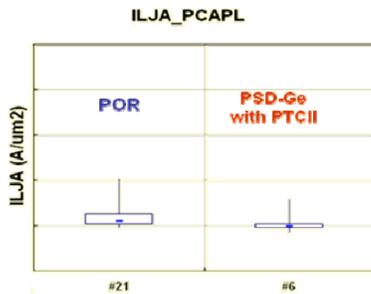


Fig. 9. Junction leakage comparison between RT and cryo implants for pSD.

#### IV. SUMMARY

In this paper, we have shown that the use of cryo implant on pSD 28nm eSiGe PMOS enables reduction of strain relaxation. SIMS profiles showed that less dopant diffusion

relative can be achieved with cryo-implantation. In addition, this study clearly showed that cryo-implantation reduces damage formation and therefore reduce junction leakage reduction.

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