Formation of Highly Reliable Cu/Low-k Interconnects by Using CVD Co Barrier in Dual Damascene Structures

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***Abstract*— CVD Co film was investigated as an alternative barrier layer to the conventional PVD TaN\Ta in V1\M2 structure for 32nm node. We improved via filling performance and upstream (V1→M2) electromigration (EM) lifetime by more than three times. Excellent step coverage of CVD barrier makes it possible to reduce the thickness of the barrier metal by 30% and to increase the volume of Cu in metal lines. RC delay also reduced with decrease in resistance. Since adhesion at the interface between the barrier-Co and Cu also is strong, migration of Cu atoms is dramatically slowed down. EM in the via is finally deterred due to absence of pre-existing voids, consequently lifetime increases. This CVD Co process is expected to be beneficial for the next technology generation beyond 20nm node.**

Keywords-Electromigration (EM), BEOL, Dual Damascene, Cu, CVD, Co

I. INTRODUCTION

While the width of metal lines has been gradually decreased every generation, the concerns about EM reliability as well as Cu filling have been increased. The grain size of Cu becomes smaller and smaller in narrow lines and consequently the diffusion path increases through the grain boundaries. Besides, high current density also contributed to accelerating Cu migration.

BEOL process of the logic devices consists of multiple layers of the dual damascene interconnect with fragile low-k inter-metal-dielectric (IMD), therefore, there are some problems associated with patterning, filling performance and reliability. So, many studies have been continuously conducted to solve them. It has been reported that migration of Cu atoms has been controlled by metal doping [1,2]. Doped species are known to interrupt the diffusion path by segregating at Cu grain boundaries. However, this method gave rise to higher resistance. Recently, CVD Ru and Co barriers have been actively studied as a next candidate, and showed a lot of promising results in filling properties, resistance and reliability [3-5].

EM is the result of the movement of Cu atoms due to an electron wind caused by an externally applied electric field. The rate of this movement varies with how fast Cu atoms migrate on a sub-layer. Stress accumulation during electromigration of Cu atoms causes void nucleation at the cathode end, and the void grows to cause a fatal failure. Void growth is predicted by calculating net atomic flux around the void with a boundary condition that assumes no flux into the void since the void is located at the cathode end [6]. Time to failure is predicted and extrapolated using a model developed by Black [7]. Most voids are commonly generated at the interface between a top of Cu line and an upper capping dielectric due to the lowest activation energy for Cu diffusion (0.9eV). Thus, a number of studies have been published that selective deposition of thin metal on Cu lines can prevent this movement [8-10].

EM is divided into upstream (V1→M2) and downstream (V2→M2) by the direction of current flow in a dual damascene structure, as shown in Fig. 1. It is natural that voids originate at the interface of Cu and capping layer regardless of the current flow (Fig. 1 a,b). If it is difficult to obtain a void-free via due to small pitch, a void firstly occurs in the via, not at the Cu\Capping layer interface (Fig. 1 c). The pre-existing void can readily cause open failure by electromigration while a device is in operation. This is the reason why upstream EM is more critical than downstream in a dual damascene and it is important to optimize the process by minimizing pre-existing voids in the interconnect.

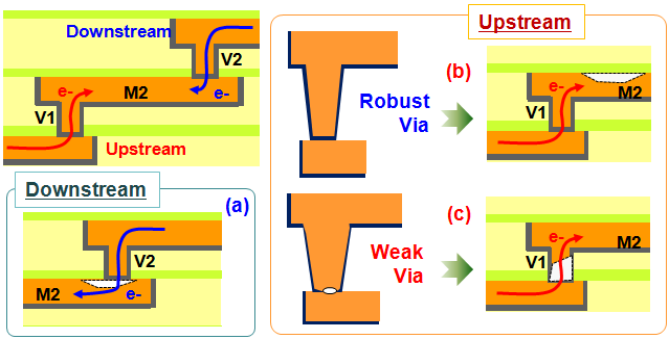

Figure 1. Two types of EM along the current flow was shown.

In this paper, CVD Co, which provides higher activation energy for Cu migration than Ta (2.0eV vs. 1.4eV) and

improved gap-fill performance, has been investigated barrier metal at V1\M2 dual damascene structure with 32nm node. The resistance and EM reliability were presented along with possible mechanism.

II. Experimental

CVD Co layer was deposited on PVD TaN by using a di-cobalt hexacarbonyl t-butylacetylene (CCTBA) precursor and hydrogen gases at 150oC. Then, hydrogen plasma treatment followed to remove C impurities which were incorporated during Co deposition. Conventional PVD seed Cu, electroplating, annealing, and CMP processes were carried out.

The split conditions of the samples for different PVD TaN thickness and stack structures are summarized in Table 1. The 32 samples per split were tested with a current density of 1.2MA/cm2 at 300°C. Resistance of each sample was monitored throughout the test. Failure was assumed if the resistance increase exceeded 10% of the initial resistance, and the current is no longer applied to the test line. Finally, the failure analysis was carried out by FIB and TEM.

TABLE I. Three Barrier Conditions Used in This Study

Sample group	1 Without CVD Co	2 With 2nm-CVD Co	3 With 2nm-CVD Co
Stack	PVD TaN\Ta	PVD TaN1 \CVD Co	PVD TaN2 \CVD Co
Normalized total thickness	1	0.81	0.73

III. Result and Discussion

A. *Step overage of CVD Co barrier*

We optimized the process of CVD Co deposition in order to obtain smooth and continuous thin film with the lowest resistance [12]. Continuous thin film of 2nm-thickness could be successfully formed in oxide trenches with the aspect ratio of 4:1. The step coverage and the distribution for Co were analyzed with scanning transmission electron microscopy-energy dispersive spectrometer (STEM-EDS) and conformal step coverage was observed as shown in Fig. 2.

B. *Gapfill and Resistance by CVD Co barrier*

Optimized stack of TaN\Co was deposited on V1\M2 low-k structure (k~2.7). The use of TaN\Co barrier stack in lieu of TaN\Ta showed a remarkable decrease in the total number of void defects after CMP to 1/15 of TaN\Ta barrier stack as shown in Fig. 3 and also revealed an about 10% decrease in line resistance while showing similar chain via resistance (Fig. 4). The lower resistance is probably attributed to the thinner barrier and the correspondingly increased Cu volume. Fig. 5 shows RC curve for TaN\Ta and TaN\Co stacks and about ~10% decrease in the RC value was also observed when a TaN\Co stack was applied.

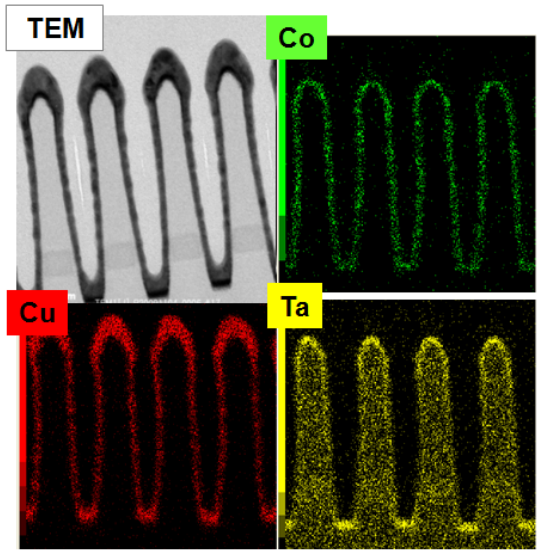

Figure 2. Almost 100% step coverage of CVD Co could be obtained in cross sectional STEM-EDS images of TaN\Co\Cu seed.

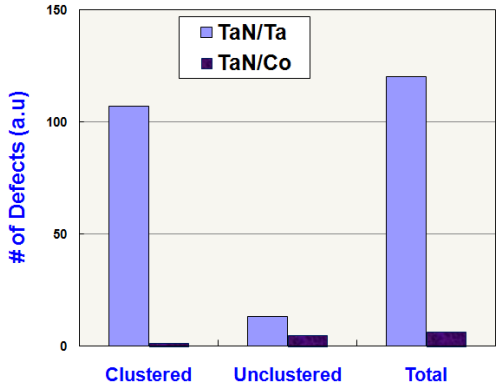

Figure 3. Classified numbers of defects after CMP was significantly decreased by using TaN\Co barrier.

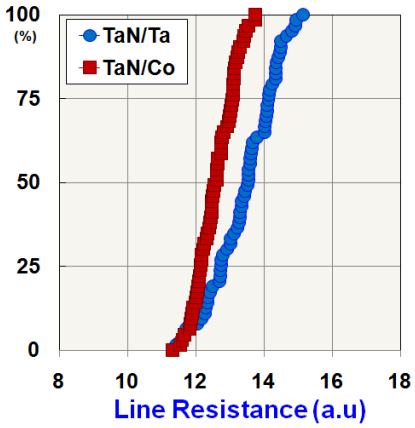

Figure 4. About 10% decrease in line resistance was seen in TaN\Co samples.

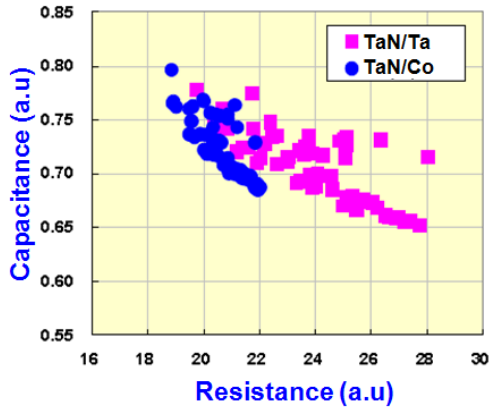

Figure 5. RC value decreased by 10% with the resistance when a TaN\Co stack was applied.

C. *Resistace gradation trend during Electromigration*

When CVD Co barrier was adopted, two different trends of resistance degradation were observed in upstream EM graph. Firstly, MTTFs (median time to failure) of CVD Co groups were increased by three times of the reference's group as shown in Fig. 6. Secondly, some CVD Co samples show gradual increases in resistance, contrary to the abrupt increase in case of PVD TaN\Ta. The gradual increment of resistance for TaN\Co barrier has been known to result from the growth of voids. Since TaN\Ta barrier has high resistivity, the current flow might be stopped when voids nucleate or grow. However, Co layer can act as a shunting layer even after a void formation due to a relatively low resistivity, and endure until it reached to a final failure size.

The physical limitation of PVD barrier is shown in Fig. 7. We can see that the thickness of PVD TaN\Ta layer depends predominately on the profile of the sub-layer. Very thin or even discontinuous layers (dashed red arrows) were observed along with the normal coverage (blue solid arrows). Due to the intrinsic asymmetric deposition in PVD system and variation of etching\deposition ratio over the wafer, it is difficult to achieve a uniform deposition of barrier metals on the surfaces with negative or 45°-tilted slope. If the coverage of barrier metal and seed Cu is insufficient, multiple micro voids would form during the subsequent electroplating process (Fig. 7 b).

D. *EM failure mechanism*

Lognormal plot (Fig. 8) helps us see the enhanced lifetime clearly. All time to failures (TTFs) of the TaN\Co group were shifted three times longer than those of the TaN\Ta, regardless of TaN thickness.

In order to understand the role of CVD Co barrier in EM failure mechanism, focused ion beam (FIB) analysis was performed for the samples with the whole range of lifetime that were plotted in Fig. 8. All of voids were observed in the via in the TaN\Ta samples, which might be related with a lack of barrier coverage as mentioned above. This phenomenon is similar to the CVD Co samples. However, other samples (Fig. 8, 9 f,g) showed voids in the M2 line, not in the V1 via. These showed longer TTF and it is believed to be a major factor for increased EM lifetime. It is the prominent evidence that robust via can be achieved by adopting CVD Co barrier and thus enhance the EM lifetime. The voids are bigger in the samples with Co than those without it. Even the void occurred in the via, it grows towards the direction of M2 line. This means that killer void which cause open failure is larger with Co barrier.

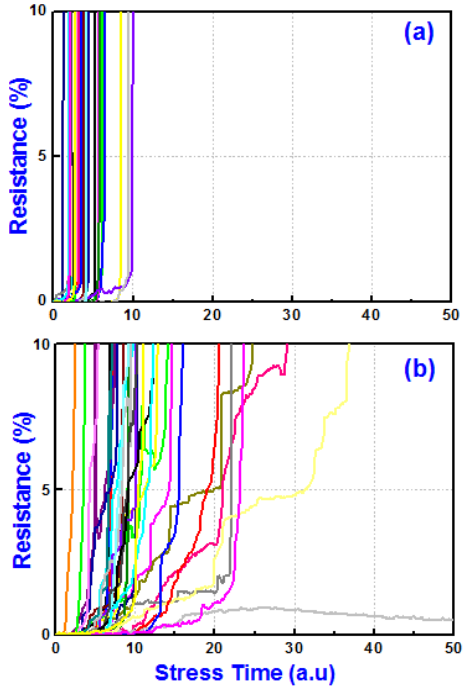

Figure 6. For upstream EM, resistance degradation trends are quite different between two groups ; (a) TaN/Ta, (b) TaN/CVD Co. When CVD Co barrier was adopted, increased MTTFs (median time to failure) and gradual increase in resistance were observed.

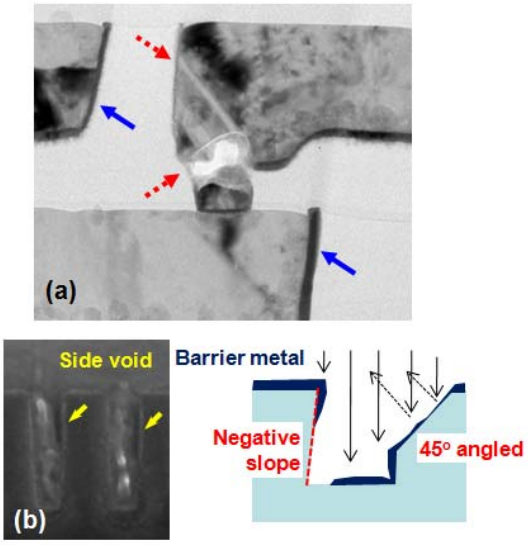

Figure 7. (a) Very thin or discontinuous layers (dashed red arrows) were observed along with the normal coverage (blue solid arrows) in TEM image of PVD TaN\Ta sample after EM test.
(b) Vertical SEM image shows the voids during elecroplating due to insufficient coverage of barrier metal and seed Cu.

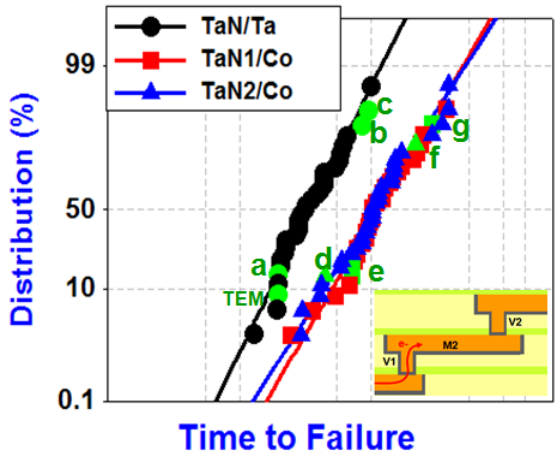

Figure 8. Lognormal probability plot of upstream EM show the enhanced lifetime clearly.
* Green samples were characterized by FIB and TEM in Fig. 7, 9.

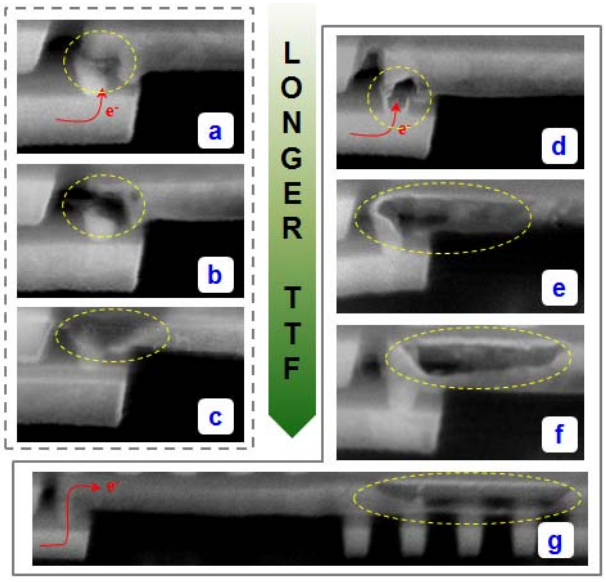

Figure 9. FIB analysis was performed for the samples with the whole range of lifetime that were plotted in Fig. 8; (a)-(c) : TaN/Ta, (d)-(g) : TaN/CVD Co

In case of a downstream (V2→M2) structure, we could not observe the shift of TTF like the upstream. It means the failure mechanism did not change and FIB images also confirmed that all of voids show the same trend for both TaN\Ta and TaN\Co groups (Fig. 11). When a void is generated under the via, it gives rise to the fatal failure in a very short time. Longer lifetime would be achieved if a void nucleates in distance of the via and grows to the opposite direction. Extrapolated lifetime to operation condition based on Black's equation is expected to increase since lognormal distribution became stiff by removal of early failures when CVD Co barrier was involved. This comes from enhanced fill performance and eliminates pre-existing voids prior to EM stressing. The vulnerable point for void nucleation was found to locate at the interface of Cu line contacted under the via, at which good adhesion of CVD Co liner to Cu could hardly affect the migration. Metal capping process would be much more effective for suppressing the void nucleation.

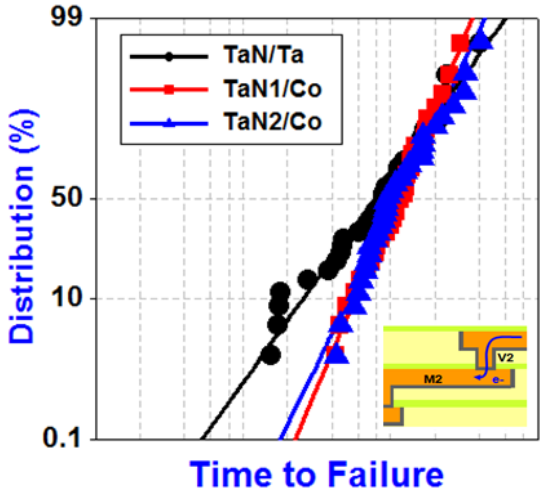

Figure 10. The shift of TTF was not observed in lognormal probability plot of downstream EM like the upstream, but the distribution became stiff by removal of early failures when CVD Co barrier was involved.

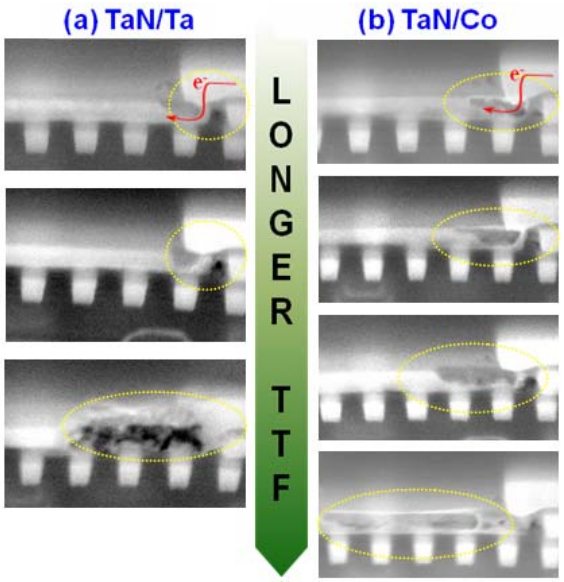

Figure 11. In FIB images, all of voids show the same trend for both barrier groups; (a) : TaN/Ta, (b) : TaN/CVD Co

In conclusion, we demonstrated that highly reliable dual damascene structure could be achieved by using CVD Co barrier. All properties which are required for logic device including void-free, low-resistance and better EM reliability were improved with an optimized condition of CVD Co process. It reduces the thickness of the barrier by 30%, and helps void-free Cu filling due to large opening. Then, EM in the via is deterred due to absence of pre-existing voids, consequently lifetime increases.

The importance of CVD barriers will be focused more and more, because the imperfect filling issue becomes more serious with the advanced technology node. In this study, we found that the use of CVD Co barrier dramatically enhanced EM lifetime by formation of robust via in a dual damascene structure due to its excellent gap-fill performance as well as better adhesion to Cu.

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