Characterization of Selectively Deposited Cobalt Capping Layers: Selectivity and Electromigration Resistance

C.-C. Yang, P. Flaitz, P.-C. Wang, F. Chen, and D. Edelstein

***Abstract*—Co films were selectively deposited as Cu capping layers by chemical-vapor-deposition technique. X-ray fluorescence spectroscopy determined the Co deposition selectivity as a function of the deposition temperature and substrate materials. The Co/Cu interfacial property was characterized and revealed no detectable oxygen at the interface. The selectivity of the Co deposition process and the property of the resulted Co/Cu interface were further confirmed with time-dependent-dielectric-breakdown and electromigration tests.**

***Index Terms*—Chemical vapor deposition, cobalt, reliability.**

I. Introduction

ELECTROMIGRATION (EM) lifetimes drop rapidly due to a scaling phenomenon and reduction of critical void size for failure as Cu interconnect feature sizes continue to shrink in nanoelectronic applications. Although the fast diffusion path in the Cu interconnects varies depending on the overall integration scheme and materials used for chip fabrication, it has been observed that Cu atoms transported along the metal/dielectric cap interface play a critical role on the EM lifetime projection. The interface between the dielectric capping layer and the Cu line represents a location that is susceptible to EM-induced mass flow [1], and this fast Cu diffusion path can be effectively suppressed by capping the Cu line with a metal capping layer [2]. While various alternate metal capping approaches have been proposed to reduce Cu transport and void growth [2]–[4], virtually all involve a tradeoff between EM improvement and Cu resistivity increase. Additional liabilities may include undesirable line-to-line leakages and capacitance increases [3], [5]. For instance, the implementation of a selective metal cap via electroless deposition is challenged by difficulty in preventing the contamination of the dielectric surface from the plating bath. In addition to leakage, yield degradation, and other reliability-related issues, a contaminated dielectric surface could also impact the overall interconnect capacitance. This electroless plating approach also adds processing steps, for example, pre- and postcleans, and increases wafer cost.

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II. Device Fabrication

In this study, blanket wafers were used first to check the selectivity of the chemical-vapor-deposited (CVD) Co process on Cu versus dielectrics. Three types of dielectrics were evaluated; type A is a dense dielectric, and types B and C are porous low-k organosilicate-glass dielectrics. Type-C dielectric has higher porosity than type B. The corresponding dielectric constant values are $k \sim 2.7$, $k \sim 2.4$, and $k \sim 2.2$ for type-A, type-B, and type-C dielectrics, respectively. Then, patterned wafers at the 32-nm technology node were prepared for TEM analysis of the Co-capped Cu interconnects. Patterned wafers consisting of one single-damascene Cu M1 and two dual-damascene Cu Mx levels in type-A dielectric and one Al termination level in FTEOS dielectric were also prepared for further electrical confirmation of the process selectivity and EM resistance of the resulted Co/Cu interface. The Cu diffusion barrier was deposited in a 300-mm deposition system integrated with degas, Ar^+ sputter, PVD Ta(N), and PVD Cu seed deposition chambers. Conventional Cu electroplating and chemical–mechanical polishing were performed on the patterned wafers. Selective CVD Co cap layers were then deposited on the exposed Cu interconnects, followed by a standard $SiC_xN_yH_z$ dielectric cap layer deposition, and then, subsequent wiring levels were built.

A Co-containing carbonyl precursor is used in the current study for chemical vapor deposition of Co. The Co carbonyl precursor is stored in the ampoule in an atmosphere comprising helium inert gas. A degas process at 300 °C in Ar was performed for 80 s before the Co deposition process. X-ray fluorescence spectroscopy was used to investigate the selectivity of the CVD Co deposition process between Cu and dielectric blanket substrates. Average deposited Co thicknesses of nine points across a 300-mm wafer for both Cu and dielectric substrates are shown in Table I. Two deposition temperatures, 200 °C and 250 °C, were checked in the study. The data indicate a higher Co deposition rate on Cu than that on dielectrics. As compared with the porous dielectrics, the deposition rate is decreasing on the type-A dense dielectric. The data also show a larger Co deposition rate increase on type-B and type-C porous dielectrics than on the type-A dense dielectric when

TABLE I
DEPOSITED Co THICKNESS AT VARIOUS SUBSTRATES [Å]

Deposition Time [SEC]	2x	3x	4x
Temperature: 200°C			
Cu	16	19	23
A: dense dielectric, k~2.7	0.2	0.2	0.3
B: porous dielectric, k~2.4	0.2	0.3	0.3
C: porous dielectric, k~2.2	0.3	0.3	0.4
Temperature: 250°C			
Cu	29	32	34
A: dense dielectric, k~2.7	0.2	0.2	0.2
B: porous dielectric, k~2.4	2.0	2.8	3.9
C: porous dielectric, k~2.2	3.0	3.6	6.2

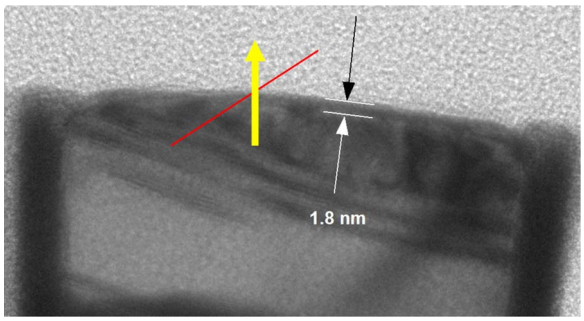

Fig. 1. Cross-sectional STEM image of a 50-nm-wide Cu line showing a smooth and uniform Co metal cap layer of ~1.8 nm.

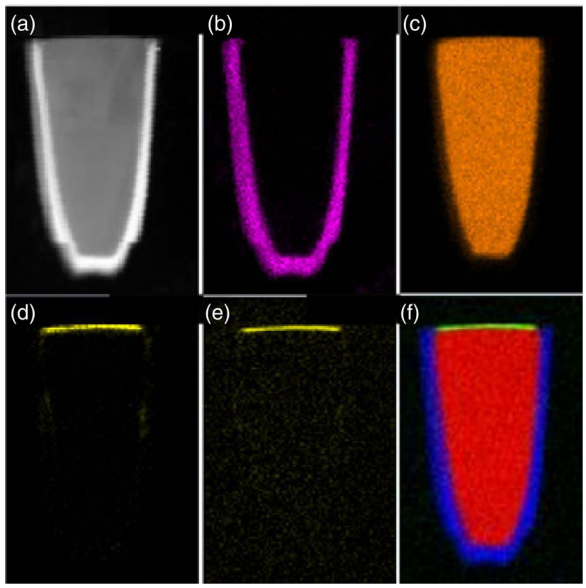

Fig. 2. (a) Cross-sectional STEM image of a Cu line capped with Co. EDX mapping showing detected (b) Ta at the sidewall of the Cu line, (c) Cu, and (d) Co at the top surface of the Cu line. (e) EELS mapping showing detected Co. (f) Color overlay [(red) Cu, (blue) Ta, and (yellow) Co] showing Co covering the entire Cu surface.

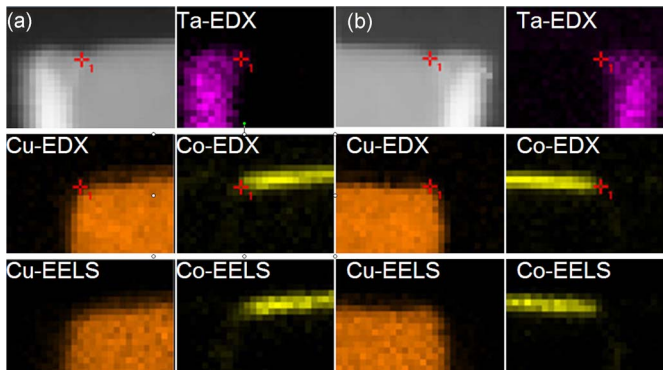

Fig. 3. EDX and EELS mapping results to assess the coverage of the deposited Co. (a) Top-left corner. (b) Top-right corner.

increasing the process temperature. As the results, the CVD Co process has better selectivity on Cu interconnects with the dense dielectric, and a 200 °C process temperature is desired for a reasonable selectivity on type-B and type-C porous dielectrics. The observed deposited Co thickness difference is attributed to the result of the difference in incubation times exhibited between Cu and dielectric substrates for the CVD Co process. The term "incubation time" is defined as the time interval between the initial exposure of the Co carbonyl precursor to the surface in question at the onset of Co deposition. The incubation time on Cu is essentially zero, while on dielectrics, it can be as large as a few minutes. During this time, a capping layer can be grown on the exposed Cu surface which does not extend onto the dielectric.

III. CHARACTERIZATION RESULTS

The representative scanning transmission electron microscope (STEM) image is shown in Fig. 1 with the metal line parallel with the electron beam direction. An ~1.8-nm Co coverage is observed atop the Cu line. Since Co has virtually no atomic number contrast relative to Cu and is very difficult to visualize, further elemental mapping analyses by both energy dispersive X-ray (EDX) and electron energy-loss spectroscopy (EELS) are performed to detect and visualize the Co capping layer at the top Cu surface, as shown in Fig. 2. A color overlay (Cu—red, Ta–blue, and Co–yellow) [Fig. 2(f)] clearly shows the Co extending over the entire $SiC_xN_yH_z$/Cu interface. The results also show no detectable nucleation of Co on the exposed dielectric. To better assess the coverage of the Co, EDX/EELS maps at 1-nm spatial resolution were obtained at the upper corner of a line, as shown by the red outline in the STEM image shown earlier. The maps shown in Fig. 3(a) have a marker indicating the same location in each map. The maps show that the Co extended to the edge of the Ta. The mapping was repeated at the opposite corner, as indicated earlier. The results are shown in Fig. 3(b). Again, the markers in the map indicate the same location and show that the Co covers the surface of the Cu up to the Ta liner. In order to further characterize the $SiC_xN_yH_z$/Co/Cu interfacial properties, an EDX/EELS line profile was obtained along the red line in the STEM image (Fig. 1), with the data replotted as if taken perpendicular to the $SiC_xN_yH_z$/Cu interface (yellow arrow). This allows for more data points without damaging the structure. Profiles for Cu, Si, Co, O, N, and C are shown in Fig. 4. The profiles show a small amount of O at the $SiC_xN_yH_z$/Co interface within the $SiC_xN_yH_z$. The amount of O is in the range of that normally detected for typical $SiC_xN_yH_z$ cap interfaces. No detectable O is observed at the Co/ Cu surface.

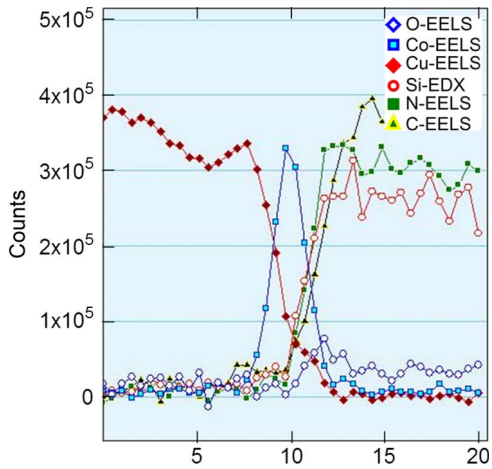

Fig. 4. EDX and EELS line profile from the $SiC_xN_yH_z/Co/Cu$ interface revealing no detectable O at the Co/Cu surface.

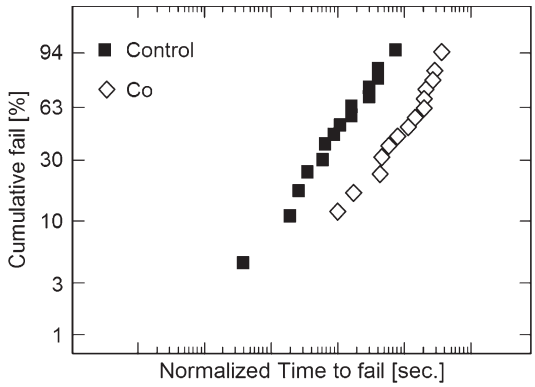

Fig. 5. Comparable distribution of TDDB fails between samples with and without Co metal cap.

Module-level time-dependent dielectric breakdown (TDDB) testing was performed to further confirm no interline problems from the CVD Co capping process. This test was carried out in an M1 comb-serpentine structure with ∼50-nm-wide lines and spaces. The dielectric between two metal lines was subjected to a constant electrical bias of 30 V at 150 °C for ∼25 h while monitoring leakage current between the two lines. The failure criterion was a leakage current > 1 μA. As compared with the control wafer, no performance degradation of TDDB stress was observed from the Co-capped wafer (Fig. 5). These data further demonstrate a good selectivity of the CVD Co metal cap process for Cu interconnects.

In order to confirm the Co/Cu interfacial property for use in the Cu interconnects, an EM evaluation was checked in a structure consisting of Cu contact plugs and a 200-μm-long ∼55-nm-wide Cu line located below. The testing was performed under a constant current density of 25 mA/μm^2 at 295 °C. Failure was defined as a 20% resistance change, and the failure distribution was assumed to be lognormal. Fig. 6 shows the representative failure distributions for the control and Co capped samples. The data indicate EM resistance enhancements for the Co-capped Cu interconnects.

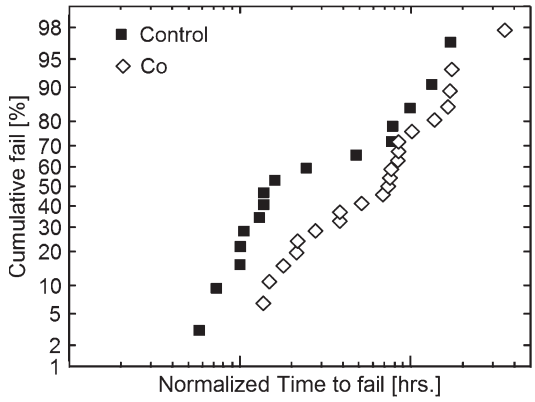

Fig. 6. Distribution of EM fails. The failure distribution from the samples with Co metal cap shows longer median time to fail.

IV. Conclusion

In summary, smooth and uniform Co films were selectively deposited as Cu capping layers by CVD. The process at 250 °C results in higher Co deposition rates at both Cu and dielectric substrates than those at 200 °C. Compared with Cu/porous dielectric, the CVD Co process shows higher selectivity between Cu and dense dielectric. $SiC_xN_yH_z/Co/Cu$ interfacial properties were characterized and revealed a small amount of O at the $SiC_xN_yH_z/Co$ interface within the $SiC_xN_yH_z$. The amount of O is in the range of that normally detected for typical $SiC_xN_yH_z$ cap interfaces, and there is no detectable O observed at the Co/Cu surface. Comparable TDDB resistance to the control and observed EM enhancement further confirm the selectivity of the Co deposition process and the resulted Co/Cu interfacial property, respectively.

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References

[1] J. Tao, N. W. Cheung, and C. Hu, "Electromigration characteristics of copper interconnects," *IEEE Electron Device Lett.*, vol. 14, no. 5, pp. 249–251, May 1993.

[2] J. R. Lloyd, M. W. Lane, E. G. Liniger, C.-K. Hu, T. M. Shaw, and R. Rosenberg, "Electromigration and adhesion," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 1, pp. 113–118, Mar. 2005.

[3] M. Tagami, N. Furutake, N. Inoue, E. Nakazawa, K. Arita, and Y. Hayashi, "Highly-reliable molecular-pore-stack (MPS)-SiOCH/Cu interconnects with CoWB metal-cap films," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2009, pp. 11–13.

[4] C.-C. Yang, F. R. McFeely, P.-C. Wang, K. Chanda, and D. C. Edelstein, "Selective chemical vapor deposition-grown Ru for Cu interconnect capping applications," *Electrochem. Solid-State Lett.*, vol. 13, no. 5, pp. D33–D35, Mar. 2010.

[5] S. Y. Chang, C. C. Wan, and Y. Y. Wang, "Selectivity enhancement of electroless Co deposition for Cu capping process via spontaneous diazonium ion reduction," *Electrochem. Solid-State Lett.*, vol. 10, no. 5, pp. D43–D46, Feb. 2007.